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Description

[METHOD OF MANUFACTURING A LOW TEMPERATURE POLYSILICON FILM]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no. 92107061, filed March 28, 2003.

BACKGROUND OF INVENTION

[0002] Field of the Invention

[0003] The present invention relates to a low temperature polysilicon film. More particularly, the present invention relates to a method for controlling the nucleation position of the crystallization of the low temperature polysilicon film.

[0004] Description of the Related Art

[0005] In the development of the process of the thin film transistor (TFT) liquid crystal display (LCD), a technology of low temperature polysilicon TFT has become a trend in recent years. The technology of low temperature polysilicon TFT

is a novel TFT technology compared with conventional amorphous silicon TFT. The electronic mobility of the novel TFT technology has been at least up to 200 cm^2/V-sec, and therefore the size of the chip area is reduced and the aperture ratio is increased. Moreover, because of the enhancement of the electronic mobility of the novel TFT technology, a part of the driving circuit can be manufactured on the glass substrate along with the TFT manufacturing process. Thus the cost of the novel TFT technology is much lower than that of the conventional amorphous silicon TFT. In addition, because the LCD produced with the low temperature polysilicon TFT has a thinner thickness, a lighter weight and a higher resolution in comparison with the LCD produced with conventional amorphous silicon TFT, the novel technology is especially applicable for electronic products that are power saving, handy, and portable.

[0006] In the conventional manufacturing process of the low temperature polysilicon TFT, the manufacturing method of the low temperature polysilicon film includes the steps of forming an amorphous silicon layer on the substrate by a chemical vapor deposition (CVD) method and of directly proceeding with a laser crystallization process. However,

the nucleation position of the crystallization process is not under control in the conventional laser crystallization process of transforming the amorphous polysilicon film to the polysilicon film. In addition, the grain sizes of the crystal are not uniform after the laser crystallization process, thus the number of grain interfaces in the channel of each TFT will be different, and if the number of grain interfaces in the channel is too large, the electric property and the stability of the TFT will be reduced.

SUMMARY OF INVENTION

[0007] Accordingly, one object of the present invention is to provide a manufacturing process of low temperature polysilicon TFT in which the position of the crystal grain is controlled by controlling the position of the crystal seed during the nucleation process of the amorphous silicon film.

[0008] It is another object of the present invention to provide a manufacturing process of low temperature polysilicon TFT in which the uniformity of the grain size and the grain distribution in the conventional manufacturing process can be resolved.

[0009] It is another object of the present invention to provide a manufacturing process of low temperature polysilicon TFT in which the number of grain interfaces in the channel of

the TFT can be reduced and the number of grain interfaces in the channel of the TFT can be controlled in a predetermined range of all of the TFTs.

[0010] In order to achieve the above objects and other advantages of the present invention, a manufacturing method of low temperature polysilicon film is provided. The method comprising the steps are described below. First, forming a first metal layer on a substrate in which a plurality of openings contiguous to the substrate is formed in the first metal layer. Second, forming a second metal layer on the first metal layer by performing an oblique evaporation step in which a hole is formed in the second metal layer corresponding to each of the openings. Third, forming a silicon layer on the second metal layer in which a silicon seed is formed on the substrate inside each of the holes. Fourth, removing the first metal layer and the second metal layer. And then forming an amorphous silicon layer on the substrate by using the silicon seed for performing a deposition process. And finally, transforming the amorphous layer to a polysilicon layer by performing a crystallization step.

[0011] In order to achieve the above objects and other advantages of the present invention, a method of controlling a

crystal seed position is provided. The method comprising the steps are described below. First, forming a first metal layer on a substrate in which a plurality of openings contiguous to the substrate is formed in the first metal layer. Second, forming a second metal layer on the first metal layer by performing an oblique evaporation step in which a plurality of holes are formed in the second metal layer corresponding to the plurality of openings. Third, forming a crystal seed layer on the second metal layer in which a silicon seed is formed on the substrate inside each of the holes. And finally, removing the first metal layer and the second metal layer.

[0012] Accordingly, because the position of the crystal seed is effectively controlled, the nucleation position of the crystal grain during the crystallization process can also be controlled.

[0013] Furthermore, because the grain size and the grain distribution can be controlled, the number of grain interfaces in the channel of the TFT can be reduced, and the electric property and the stability of the TFT will be enhanced.

[0014] It is to be understood that both the foregoing general description and the following detailed description are exemplary and are intended to provide further explanation of

the invention as claimed.

Brief Description of Drawings

[0015] The accompanying drawings are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0016] FIG. 1A to FIG. 1G schematically illustrate the cross-sectional diagrams of a manufacturing process flow of low temperature polysilicon film of a preferred embodiment of the present invention.

[0017] FIG. 2 is a top view schematically illustrating the photo resistant layer shown in FIG. 1.

Detailed Description

[0018] The present invention now will be described more fully hereinafter with reference to the accompanying drawings in which preferred embodiments of the invention are shown. The present invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be

thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout. Moreover, each embodiment described and illustrated herein includes its complementary conductivity type embodiment as well.

[0019] The present invention provides a manufacturing method of low temperature polysilicon film. FIG. 1A to FIG. 1G schematically illustrate the cross-sectional diagrams of a manufacturing process flow of low temperature polysilicon film of a preferred embodiment of the present invention. Referring to FIG. 1A, there is provided a substrate 100 first, the material of the substrate 100 includes, but is not limited to, glass or plastic. Second, there is formed a first metal layer 106 on the substrate 100. In a preferred embodiment of the present invention, the first metal layer 106 is composed of, for example but not limited to, a bottom metal layer 102 and a top metal layer 104.

[0020] After that, a photo resistant layer 108 is formed on the first metal layer 106 in which an opening pattern 108a is formed in the first metal layer. If the present invention is provided for a manufacturing method of low temperature polysilicon TFT of LCD, the top view of the photo resistant layer 108 may be similar to the diagram shown in FIG. 2 in

which the arrangement of the opening pattern 108a is arranged in a regular array.

[0021] Referring to FIG. 1B, an opening 110 contiguous to the substrate 100 in the first metal layer 106 is formed by etching the first metal layer 106 using the photo resistant layer 108 as an etching mask. Thus, a patterned first metal layer 106 composed by the patterned bottom metal layer 102a and the patterned top metal layer 104a is formed.

[0022] Thereafter, the oblique evaporation step 112 is performed for forming a second metal layer 114 on the patterned first metal layer 106a in which a hole 116 is formed in the second metal layer 114 corresponding to the opening 110 as shown in FIG. 1B and FIG. 1C. The oblique evaporation step 112 includes, but is not limited to, an electron beam evaporation step, and an oblique angle 112a of the oblique evaporation step 112 is, for example but not limited to, in a range of about 10 degrees to 30 degrees, 20 degrees being preferable.

[0023] In a preferred embodiment of the present invention, a material of the second metal layer 114 is the same as a material of the patterned bottom metal layer 102a of the patterned first metal layer 106a. This is preferred because

the same etching solvent can be used to etch the second metal layer 114 and the patterned bottom metal layer 102a of the patterned first metal layer 106a. Therefore, both the second metal layer 114 and the patterned first metal layer 106a can be removed simultaneously.

[0024] Here, the material of the bottom metal layer 102 includes, but is not limited to, aluminum; the material of the top metal layer 104 includes, but is not limited to, chromium; and the material of second metal layer 114 includes, but is not limited to, aluminum.

[0025] Referring to FIG. 1D, a silicon layer 120 is formed on the second metal layer 114; and a silicon seed 120a is formed on the substrate 100 inside the hole 116. The size of the silicon seed 116 is in a range of about 0.5 μm to 1.0 μm. In a preferred embodiment of the present invention, the method of forming the silicon layer 120 includes, but is not limited to, an electron beam evaporation method 118.

[0026] Here, the silicon seed 120a is formed on the substrate 100 inside the hole 116 as shown in FIG. 1C. And the hole 116 is formed corresponding to the opening 110 as shown in FIG. 1B. Therefore, by controlling the position of the opening 110 in the patterned first metal layer 116a, the position of the silicon seed 120a can be controlled

exactly.

[0027] Referring to FIG. 1E, the patterned first metal layer 106a and the second metal layer 114 are removed, and only the silicon seed 120a remains. If the materials of both the patterned bottom metal layer 102a and the second metal layer 114 is, for example, aluminum, a method of removing both of the second metal layer 114 and the patterned first metal layer 106a includes, but is not limited to, a method by using a phosphoric acid.

[0028] Referring to FIG. 1F, an amorphous silicon layer 122 on the substrate 100 is formed by using the silicon seed 120a for performing a deposition process. In a preferred embodiment of the present invention, a method of forming the amorphous silicon layer 122 includes, but is not limited to, a chemical vapor deposition (CVD) method. And a thickness of the amorphous silicon layer 122 formed is in a range of about 30 nm to 70 nm, 50 nm being preferable.

[0029] Referring to FIG. 1G, the amorphous layer 122 is transformed into a polysilicon layer 122a by performing a crystallization step. In a preferred embodiment of the present invention, the crystallization step includes, but is not limited to, a laser crystallization step.

[0030] Here, because the amorphous layer 122 is formed by using the silicon seed 120a as a seed during the crystallization process, the position of the silicon seed 120a can be controlled precisely by the method described above in the preferred embodiment of the present invention. Thus, the nucleation position can be controlled after the crystallization step.

[0031] Here, if the present invention provides for a manufacturing method of low temperature polysilicon TFT of LCD, the position of the crystal grain is controlled by controlling the position of the crystal seed by using the method provided in the invention. Therefore, the number of grain interfaces in the channel of the TFT can be reduced, and the number of grain interfaces in the channel of the TFT can be controlled in a predetermined range of all of the TFTs.

[0032] In the embodiment of the present invention, the position of the crystal grain of the low temperature polysilicon film is controlled by controlling the position of the crystal seed. However, the method of the controlling the position of the crystal seed by using the oblique evaporation method may not only provide for a manufacturing method of low temperature polysilicon film, but also provides for

another method of manufacturing a thin film.

[0033] Accordingly, because of the position of the crystal seed is effectively controlled, the nucleation position of the crystal grain during the crystallization process can also be controlled.

[0034] Furthermore, the grain size and the grain distribution can be controlled, and the number of grain interfaces in the channel of the TFT can be reduced, and the electric property and the stability of the TFT will be enhanced.

[0035] It will be apparent to those skilled in the art that various modifications and variations can be made to the features of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations thereof provided they fall within the scope of the following claims and their equivalents.